Solid-State 8GHz Transient Signal Digitizer Characterization

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***Abstract* — A new technique leading to an accurate sampling of single shot high frequency signals is described. This technique provides 20GHz sampling of electrical pulses up to 8GHz bandwidth with a 60dB dynamic range. The prototype of a transient digitizer involving this new principle is tested, with the goal of a new product development.**

We present the theory of the sampling operations, the outline of the prototype, the design and fabrication of an innovative set of specific GaAs MMICs, the assembling of the complete system and the first results obtained in performances characterization.

I. Transient Digitizers

Many experimental domains such as lasers, nuclear, radars or telecommunications optics deal with ultra fast phenomena and require real-time measurements of instantaneous pulses. Recording a short duration single-shot signal, with a large dynamic, is still a technical and economical challenge.

Digitizers usually couple a fast sensor, a stack memory, and an analog to digital converter. Fast cathode ray tubes stores a global analog information before sampling and digitizing [1]. Present real time scopes sample the signal as fast as they can digitize and store data [2].

We propose here a spatial sampling technique, based on a large set of elementary samplers. First, each of them samples an analog part of the signal according to the sampling rate; then, in a second phase, digital conversion and numeric storage are operated. This loosens time, allows careful operations on data, and provides the results with a large dynamic range.

II. Spatial Sampling

The analog signal under analyze is brought to the input of each elementary sampler via an adapted propagation structure that preserves its temporal figure in the considered bandwidth. The elementary samplers are distributed along this propagation structure [3]. Each of them can observe the signal variations at a specific instant, the equivalent delay between two successive samplers depends on their pitch and on the wave velocity in the transmission structure (fig. 1).

The elementary sampler operates at reception of a trigger command. This command is a logical signal. It can

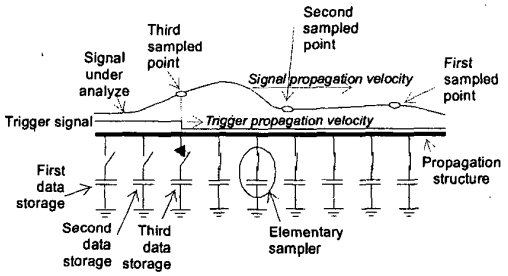

Fig. 1. spatial sampling schematic description

be propagated from sampler to sampler with a controlled delay. The sampling period of the digitizer is set by this controlled trigger delay, minus the signal propagation delay between samplers [4].

This technique allows analysis over a longer temporal window than the actual equivalent propagation time on the transmission line. The distortion of the signal under analyze is thus minimized. The sampling frequency and the analysis window are ajustable by modifying the trigger propagation delay between elementary samplers.

III. Goal Specifications And Preliminary Demonstrator

Using this principle, we mean to develop a digitizer for single shot signals with a bandwidth as high as 8GHz, with a 60dB dynamic range, with a sampling frequency up to 20GHz. The number of samples proposed is set to 100 in a first approach, open to be increased.

The feasibility and performances of such a device have to be proved at first. For this purpose, we realized a demonstrator with a number of elementary samplers limited to 24. The analysis window of the demonstrator is 1ns long for the Ultrafast channel.

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IV. CIRCUITS IMPLEMENTATION

Sampling operations needs for high frequency analog amplifiers and fast transitions. We decided to develop a specific set of GaAs MMIC to carry out the high frequency core of the device. We chose the OMMIC 0.2µm GaAs p-HEMT technology regarding to performances, and maturity [5][6].

A. Sampling Process Description :

The elementary sampler is to capture the voltage facing its input on the line at a specified instant, and to maintain it long enough for standard component to take over it. It is made of two sample-and-hold stages in series, each of them is in charge to increase the lifetime of the sampled data. The input is a high impedance, high frequency, voltage follower buffer, to isolate the signal line from sampling perturbation.

The first sample-and-hold, when in passing mode ("On" state), is in accordance with the signal bandwidth up to 8GHz. The storing capacitance C_1 is 0,3pF. The switch turns to the "Off" state in 20ps; its Roff/Ron ratio is about 3300. The small charge quantity stored in C_1 is the sampled data. Its lifetime is only a few tens nanosecond, still too short. A second sample-and-hold stage is added, to sample the voltage of C_1. This second stage operates at a lower frequency, with a storing capacitance C_2 equal to 10pF. The lifetime is increased to 6µs, and the data is now accessible for standard components operation. An extra output buffer protect the circuits from external hazards.

Two internal trigger signals are necessary to operate the two successive sampling operations in each sampler. The first trigger actually selects a data from the analog signal. The second trigger is delayed from the previous trigger by a few nanoseconds. This delay is optimized to preserve the final signal to noise ratio.

The analog signal under analyze and the two trigger signals have to be propagated from sampler to sampler. The triggers, as they are logical signals, are maintained and delayed by controlled inverters commutations in series.

The analog signal propagates on a 50Ω transmission line section between two samplers. The signal is slightly distorted though the input impedance of the samplers has been taken into account for the line calculation. To preserve the information level in the propagating signal, it is periodically restored by a adapted amplifier designed to compensate the line losses for all the frequencies with a constant group delay. Low reflection coefficients avoid stationary effects to overrun the signal.

Considering the noise figure of this amplifier, the signal-to-noise ratio along the line addressing the 100 sampler inputs is optimized when one amplifier is inserted every 12 samplers. The simulation predicts that for a 100 samplers assembly, the signal-to-noise ratio is higher than 64dB for any of them (fig. 2).

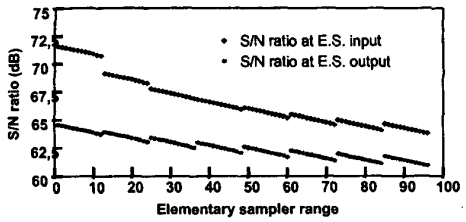

Fig. 2. Estimated signal-to-noise ratio at the input and at the output of the first 100 elementary samplers

B. GaAs Circuits Summary

The high frequency sampling set of GaAs circuits is assembled in a shielded module.

The set of GaAs circuits includes four types of MMIC :
- the "PS" circuit, for propagation and sampling circuit. The PS circuits includes a propagation line section, four elementary samplers, and the logic means for the management and propagation of the two internal triggers. These MMIC are made of 500 transistors on a 14mm² surface of GaAs substrate (fig. 3).
- the "AR", refreshing amplifier,
- a "Delay" circuits, for the triggers synchronism,
- an "Interface" circuit, responsible for generating the two internal triggers on reception of an external trigger.

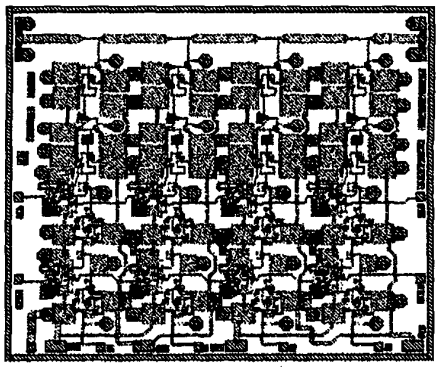

Fig. 3. Layout of a PS type circuit

The functional simulation of individual circuits, and simulation of the whole system have been run [6] with MDS and Spice simulation codes and showed good

performances in step acquisition and number of effective bits.

V. DEMONSTRATOR ASSEMBLY

The circuits are assembled (fig. 4) in a shielded module box (fig. 5).

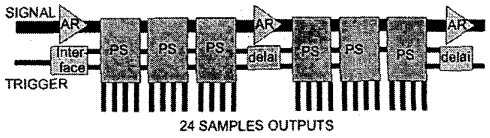

Fig.4. GaAs circuits assembly for the demonstrator sampling module.

The modules are fitted into a surrounding equipment designed to demonstrate the sampling performances with a

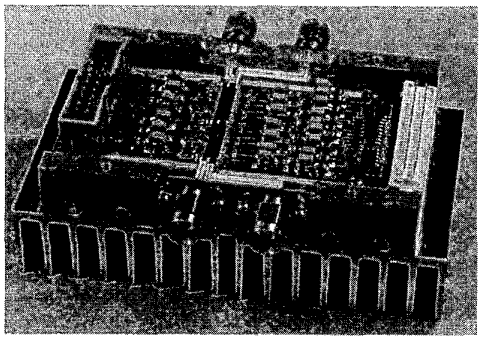

Fig. 5. Open sampling module box, including GaAs circuits assembly and bias filters, with connectors and radiator.

minimum of external hazards.

This equipment first realizes the analog storage of the data read from the outputs of the GaAs elementary samplers into a set of standard sample-and-hold circuits. Then they are sequentially read, amplified, transmitted to a PC, and converted by a standard 12 bits acquisition board plugged into the computer. The logical sequence and the timing of operations are locally controlled by an EPLD device. The whole acquisition configuration is set from the PC via a driving software. The data are converted into volts and seconds referring to previous calibration values, and available for visualization and further processing.

VI. PERFORMANCES MEASUREMENTS

We present the results obtained for the whole setting : the data considered have flown from the input signal through the GaAs circuits, the readout electronics, the cable towards the computer, and have been digitized.

A. Preliminary settings :

The readout electronic by itself has a noise of 0.8LSB, measured by injecting a DC voltage in place of the GaAs samplers output.

The gain is roughly homogeneous among GaAs elementary samplers over the input voltage range; each of them however affects its data output with a specific offset voltage. The analog-to-digital conversion range is common to all of them, so a specific sampler output data range don't lay over the whole binary scale.

B. DC measurements

The noise measured for each of the sampling gates for a voltage ranging from –0.5V to 0.5V is lower than 1mV rms. Over that voltage range, an average dynamics of 63dB is achieved. Linearity is performed through a voltage calibration (fig. 6).

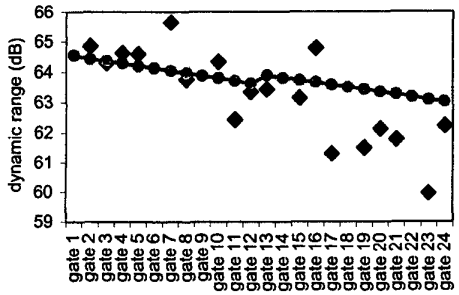

Fig. 6. Dynamics measured on each of the operational sampling gates (black dots) compared with the theoretical dynamics (grey line).

C. Sampling moment calibration

A pure sine wave is injected in the signal input, and acquisitions are asynchronously run. For each acquisition, a reverse time calculation is operated, gate by gate, to fit with the ideal sine waveform. Samples corresponding to a sine phase close to $\Pi/2$ or $3\Pi/2$ are moved apart as they lack in precision. The calculation process is repeated over many acquisitions. This calibration is reproducible with a standard deviation of 0.5ps on the sampling moments.

The average delay between moments is 57ps, corresponding to a 17.5GHz sampling frequency.

D. Measurement bandwidth

We measure the bandwidth of the digitizer with a frequency synthesizer connected to the signal input. The envelope of the data for each sampling gate over a large number of acquisitions yields to the transmission coefficient of the injected frequency. At the frequency of 8GHz, an attenuation of 4.5dB is obtained (fig. 7).

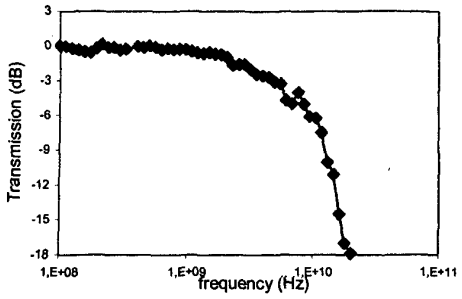

Fig. 7. Measurement Bandwidth

A second experiment was to sample the edge of a 54ps step generator. The rise time of the signal built from the samples is 100ps so the digitizer own rise time is 85ps. The rise time and the front description are similar

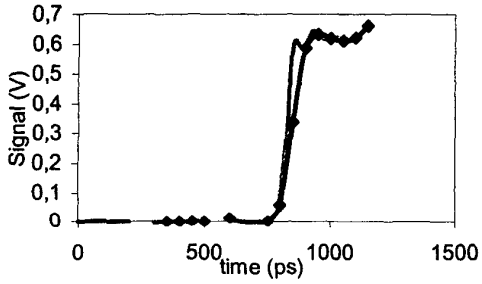

Fig. 8. Measurement of a PPL4050 step generator front by a TEK.SD24 sampling head (grey line), and by the digitizer module (black dots and line)

wherever the front is sampled on the propagation line (fig. 8).

E. Time base

The delay between the analog external trigger and the capture of the first sample is 3ns. The jitter is evaluated by the step generator front measurements lower than 10ps.

This demonstrator has been built from the first version of the GaAs circuits set. The whole unusual and complex assembly is running. Though an investigation has to be carried out to determine the cause of the excess of attenuation on the upper part of the bandwidth, most of the major questions that the spatial sampling principle rises have been answered through the characterization of this demonstrator : the measurement noise is lower than 1mV, the dynamics is about 64dB, the propagation along the line preserves the signal figure, and the sampling time sequence is reliable and reproducible.

The next step on the development is to increase the number of elementary samplers, so that actual measurement campaigns can be carried out and demonstrate the performances with use.

VII. Conclusion And Perspectives

This new generation of digitizer is based on the multiplicity of elementary systems devoted to the high frequency sampling operations. This loosens the time stress on the fast data handling and increases the measurement dynamic.

The characterization of the first demonstrator gives decisive proofs on the feasibility and interest for spatial sampling in accurate single shot measurements.

We now foresee the objective performances that could be reach in further versions : considering the available MMIC technologies, doubling the sampling rate and the signal frequency up to 16GHz is within reach.

Multiple accommodations may be scanned : increasing the number of elementary samplers, cascade or parallel arrangements of devices to modulate the record length or the sampling rate, direct optical inputs, etc.

This spatial sampling principle is potentially the core of a new series of performing, compact and low cost digitizers.

References

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